applying a voltage to a first gate of the JFET, wherein the voltage is applied from the first gate to the first p-well region; and

applying the voltage to a second gate of the JFET, with the first gate and the second gate being on opposite sides of the source region, wherein the voltage is applied from the second gate to the second p-well region, and wherein the first portion of the current is pinched-off by first depletion regions formed due to the voltage.

2. The method of claim **1** further comprising:

applying the voltage to a third p-well region, wherein the second p-well region and the third p-well region are on a same side of the source region, and wherein the second portion of the current is pinched-off by second depletion regions formed due to the voltage.

3. The method of claim **1**, wherein the first portion of the current is pinched-off by the first depletion regions growing in a first direction parallel to a source-to-drain direction of the JFET.

4. The method of claim **3**, wherein during a period of time in which the first portion of the current is pinched-off in the first direction, the first portion of the current is not pinched-off in a second direction perpendicular to the source-to-drain direction of the JFET.

5. The method of claim **3**, wherein during a period of time in which the first portion of the current is pinched-off in the first direction, the first portion of the current is further pinched-off in a second direction perpendicular to the source-to-drain direction of the JFET.

6. The method of claim **1**, wherein the second portion of the current comprises:

a first sub-portion level with the first PBL and the second PBL; and

a second sub-portion over the first PBL and the second PBL.

7. The method of claim **1**, wherein during a period of time in which the current is pinched-off by the voltage, a first depletion region grown from the first p-well region is merged to a second depletion region grown from the second p-well region, with the first depletion region and the second depletion region comprised in the first depletion regions.

8. The method of claim **1** further comprising, during the applying the voltage to the second gate, applying the voltage to a gate electrode of a Metal-Oxide-Semiconductor (MOS) device, with the MOS device comprising the source region of the JFET as a source region of the MOS device.

9. The method of claim **1** further comprising, during the applying the voltage to the second gate, applying an additional voltage to a gate electrode of a Metal-Oxide-Semiconductor (MOS) device, with the MOS device comprising the source region of the JFET as a source region of the MOS device, and wherein the voltage and the additional voltage are different from each other.

10. The method of claim **1**, wherein the voltage is an electrical grounding voltage or a negative voltage.

11. A device comprising:

a buried well region of a first conductivity type over a substrate layer;

a first High Voltage Well (HVW) region of the first conductivity type over the buried well region;

an insulation region over the first HVW region;

a drain region of the first conductivity type on a first side of the insulation region;

a gate electrode on a second side of the insulation region;

a well region in a region adjacent to the insulation region, wherein the well region is of a second conductivity type opposite to the first conductivity type;

a second HVW region of the first conductivity type in the well region, wherein the second HVW region overlaps a portion of the buried well region; and

a source region of the first conductivity type in a top region of the second HVW region.

12. The device of claim **11**, wherein the first conductivity type is n-type.

13. The device of claim **11**, wherein the well region comprises a first portion and a second portion on opposite sides of the second HVW region.

14. The device of claim **11**, wherein the well region encircles the second HVW region.

15. The device of claim **11**, wherein the well region is configured to pinch off a current flowing in the buried well region.

16. The device of claim **11** further comprising a buried well layer between the first HVW region and the buried well region, wherein the buried well layer is of the second conductivity type, and wherein the buried well layer is connected to the first well region.

17. The device of claim **11** further comprising an additional well region over the buried well region, wherein the additional well region is spaced apart from the well region by a portion of first HVW region, and wherein the first HVW region is connected to the second HVW region to form a continuous HVW region that is connected between, and contacting, the drain region and the source region.

18. The device of claim **11**, wherein the well region comprises strips having lengthwise directions parallel to a lengthwise direction of the second HVW region, and wherein the first HVW region is disconnected from the second HVW region.

19. A method comprising:

forming a buried well region of a first conductivity type over a substrate layer;

forming a first High Voltage Well (HVW) region of the first conductivity type over the buried well region;

forming an insulation region over the first HVW region;

forming a drain region of the first conductivity type on a first side of the insulation region;

forming a gate electrode on a second side of the insulation region;

forming a well region of a second conductivity type in a region adjacent to the insulation region;

forming a second HVW region of the first conductivity type between the well region, wherein the second HVW region overlaps a portion of the buried well region; and

forming a source region of the first conductivity type in a top region of the second HVW region.

20. The method of claim **19**, wherein the first conductivity type is n-type.

* * * * *